

ABSTRACT

An image processing device is provided capable of making a CPU operate efficiently to achieve overall increased speed in image processing. In an image processing device 1, a high-speed bus 10 and a peripheral bus 12 are linked via a bus bridge 11 and connected to the buses 10 and 12 are a CPU 13 for carrying out computation and control of image processing, a data transceiving FIFO memory 18 for carrying out transceiving of image compression data with a host device 4, a frame memory 16 for storing image expansion data from an electronic camera 2 and the like and displaying this data on a display panel 3, and a compression/expansion circuit 17 for carrying out compression of image expansion data and expansion of image compression data, and wherein the CPU 13 and the frame memory 16 are connected to the high-speed bus 10 and the data transceiving FIFO memory 18 is connected to the peripheral bus 12.